REMARKS

This Request for Continued Examination and Response responds to a final Office Action dated June 19, 2003. In the Office Action the Examiner rejected claims 1-17 under 35 U.S.C. §112 as failing to comply with the written description requirement. More specifically, the Examiner contends that the specification does not support a method or apparatus for exercising, connecting and optically stimulating components on integrated circuits simultaneously, as specified in the claims as amended. The Examiner contends that the specification shows only one component on an integrated circuit being exercised, connected to an electrical source and optically stimulated at a time. No claims are allowed.

Applicant responded to the final Office Action by identifying several places where, in the as-filed specification, support is provided for exercising, connecting and optically stimulating components in a large plurality of integrated circuit die on a wafer, simultaneously. The Final Office Action, dated June 19, 2003, and the Advisory Action dated October 21, 2003, both state that claims 1-17 have been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. More specifically, the Final Office Action states that, "...the specification does not have support for a method or an apparatus for exercising, connecting and optically stimulating components on the integrated circuit simultaneously as recited in recently amended claims. From the specification, it appears that there is only one component on an integrated circuit is exercised, connected to an electrical source and optically stimulated one at a time."

35 U.S.C. 112, first paragraph, states that "(t)he specification shall contain a written description of the invention, and a manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention." In the instant case, the issue is whether the present invention specification provides enough instruction to allow a person skilled in the art to use the claimed invention to simultaneously test or burn-in a plurality of integrated circuit die.

As noted in the Background of the specification, a wafer consists of a plurality of identical, yet electrically separate die. Conventionally, each die is given an initial test, and if the die passes, it is sawed from the wafer and attached to a package. A plurality of packages is then attached to a burn-in board. Several burn-in boards (i.e., 52) are then exercised in a burn-in oven. After burn-in, each die is given a final test (page 2, line 20 through page 3, line 21). Note, all page and line number references herein are to the as-filed specification, not the amended version submitted herewith. The cost associated with individually packaging and testing each die is burdensome. The specification suggests that a wafer-level test would eliminate the need to individually test each die, but notes that it would take 96,000 physically connected probes to simultaneously test each die on a wafer using conventional processes (page 5, line 4 through page 6, line 4). The present invention addresses this problem by teaching that an entire wafer of die may be tested using only a relatively few number of physical connections, with a probe board that uses fiber optical cables to introduce test signals in the form of light.

Fig. 1 describes a wafer 10 with forty-five identical, electrically isolated die 16 (page 9, lines 10-17). Details of an individual die are introduced in the explanations of Figs. 2 and 3. However, even these die-level explanations incorporate references to the invention as a wafer-level tester. For example, the specification states that the elimination of "the need for a direct physical/electrical connection to each of contact pads 18 on a die provides the following advantages: allows a wafer-level burn-in of multiple die because optical signal fibers can be placed in a tighter arrangement than electrical probes; ..." (page 15, lines 14-18). As support, the specification additionally notes that fiber optic "bundle 90 extends across the entire diameter of chamber 60 and, therefore, across the entire diameter 12 of wafer 10." (page 20, lines 17-18)

Fig. 6 is described a side view of *a section* (emphasis added) of probe card 74 and a die 16. The description states that, "(i)n the preferred embodiment, probe card 74 extends across the full diameter 12 of wafer 10 so that a single probe card is used during simultaneous burn-in of each die on the wafer." (page 23, line 21 through page 24, line 2) The probe card 74 includes moveable switches. Switch 120 is described as a "main control switch for simultaneously providing power to each die on wafer 10." (page 24, lines 21-22) Switch 120 is mentioned later, where the specification states, "(t)he portion of probe card 74 shown in Fig. 11 includes optical switch 120 for simultaneously powering on and off all the die on the water." (page 30, lines 15-16)

Simultaneous (wafer-level) die testing is described in the explanation of switch 121. Switch 121 isolates an individual die to reduce "the problem of one die shorting out the power to all other die on the wafer when all the die are electrically tested in parallel." (page 25, lines 1-3)

Likewise, lead 132 is connected through switch 121 to electrical connect individual die on wafer 10 in parallel (page 25, lines 13-16). Further, the probe card 74 is described as having 135 electrically conductive bumps (physical connections) for communication with each of the 45 die of the wafer (page 26, lines 12-14).

The above-mentioned examples are not an exhaustive list of wafer-level test descriptions. Other descriptions of a wafer-level burn-in tester that simultaneously tests a plurality of die on a wafer exist in the specification. Several of those descriptions in the as-filed specification were identified by applicant in the response filed after the final rejection and include the paragraphs of the specification amended herein. The Examiner was unpersuaded by applicant's after final submission. Accordingly, applicant has filed this RCE and amendment.

Applicant wishes to thank the Examiner for his willingness to discuss the reasons for his final rejection on the telephone with applicant's attorney, David Ripma, on December 17, 2003. In that telephone discussion the Examiner indicated that, among the quoted passages from the as-filed specification identified by applicant in his Corrected Response dated November 14, 2003, the one which he found clearest in supporting the exercising, connecting and optically simulating of multiple components on integrated circuits simultaneously appeared at page 30, lines 15-16. That passage includes the phrase ". . . simultaneously powering on and off all the die on the wafer." The Examiner preferred that language to other language, for example at page 24, lines 1-2, wherein the method is described as ". . . simultaneous burn-in of each die on the wafer." Applicant respectfully submits that either wording describes a method and apparatus which exercises plural components simultaneously. Nevertheless, Mr. Ripma

offered to amend the specification in several places to insert redundant language paralleling that on page 30, lines 15-16.

The amendments to the specification made herein include no new matter. Except in places where it would result in awkwardly redundant phraseology, applicant has added the exact words from page 30, lines 15-16, e.g., "simultaneously [exercising] *all* die on the wafer," without deleting the as-filed wording, e.g., "simultaneous [exercising] of *each* die on the wafer." Applicant's position is that the meaning is clear in both cases, i.e., the method and apparatus of the present invention allows for all the die on the wafer to be simultaneously exercised. Applicant respectfully submits that these amendments, while unnecessary, fully respond to the Examiner's objections. As such, this response overcomes the rejection under §112.

In addition to the foregoing amendments to the specification, applicant has added new claims 18-28.

As an attachment hereto, applicant is providing a substitute specification, excluding the claims, under 37 C.F.R. §1.125. In accordance with 37 C.F.R. §1.125(c), the substitute specification includes a version with markings indicating all changes and a clean version (without markings) incorporating the changes.

On November 14, 2003, applicant filed a Petition for Extension of Time Under 37 C.F.R. §1.136(a) requesting a three-month extension, together with a deposit account authorization for the fee therefore. Accordingly, the period for responding to the final Office Action of June 19, 2003, has been extended to December 19, 2003 and the present RCE and Response is timely.

In view of the foregoing, applicant requests reconsideration of the application, as amended, and submits that the application is now in allowable form and should be passed to issue.

Respectfully submitted,

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